Amendments to the claims:

1. (canceled)
2. (canceled)
3. (canceled)
4. (canceled)
5. (canceled)
6. (canceled)
7. (canceled)
8. (canceled)
9. (canceled)
10. (canceled)
11. (canceled)
12. (currently amended) An ESD protection circuit for an internal circuit that includes an I/O contact, comprising

    an ESD clamp between power rails for the internal circuit,

    a first three pin diode structure having two anodes and a cathode, connected between the I/O contact and one power rail, wherein the two anodes include an input anode connected to the I/O contact, and a separate output anode connected to the internal circuit, and

    a second three pin diode structure having two cathodes and an anode, connected between a second power rail and the I/O contact, wherein the two cathodes include an input cathode connected to the I/O contact, and a separate output cathode connected to the internal circuit.
13. (currently amended) An ESD protection circuit of claim 12, wherein the two anodes of the first diode structure are separated by an internal resistive element of the first three pin diode structure, and the two cathodes of the second diode structure are separated by an internal resistive element of the second three pin diode structure.

14. (currently amended) An ESD protection circuit of claim 12, wherein the first three pin diode structure is a p-well diode with the first anode connected to the I/O contact and the ~~a~~ second anode is connected to an input to the internal circuit and separated from the first anode by a p-well, and the cathode terminal of said first three pin diode structure is connected to a power rail, and wherein the second three pin diode structure is a n-well diode in which the first cathode is connected to the I/O contact and ~~a~~ the second cathode is connected to the input to the internal circuit and spaced from the first cathode by a n-well, and the anode of said second three pin diode structure is connected to the other power rail.

15. (original) An ESD protection circuit for protecting an input to an internal circuit from ESD current pulses to an I/O contact, comprising,

a bipolar junction transistor structure for shunting current to ground, wherein the bipolar junction transistor structure includes a first base contact connected to the I/O contact, and a second base contact connected to the input of the internal circuit, wherein the two base contacts are separated by a resistive element between the two base contacts.

16. (original) An ESD protection circuit of claim 15, wherein the resistive element includes a base polysilicon region.

17. (previously presented) A method of protecting an input to an internal circuit against ESD currentl pulses to an I/O contact, comprising

shunting the current pulse to ground by means of a bipolar junction transistor structure wherein the bipolar junction transistor structure includes a first base contact and a second base contact, and wherein the method includes connecting the first base contact to the I/O contact and the second base contact to the input of the internal circuit, and providing a resistive current path between the first base contact and the second base contact.

18. (previously presented) A method of claim 17, wherein the resistive current path comprises at least one internal resistive element of the bipolar junction transistor structure.

19. (original) A method of claim 18, wherein the internal resistive element includes a base polysilicon region to which both base contacts are connected.